A Universal Optimal Drain–Source Voltage Tracking Scheme for Synchronous Resonant Rectifiers in Megahertz Wireless Power Transfer Applications

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***Abstract*—For wireless power transfer (WPT) in mobile applications, the receiving side is usually embedded inside the devices, which makes the heating issue quite challenging, especially at high operating frequency (such as 6.78 MHz) and high power levels. High-frequency synchronous resonant rectification is expected to significantly reduce the power loss on the receiving side and thus improve the rectifier power density. This article proposes a universal optimal drain–source voltage (ODSV) tracking scheme for synchronous resonant rectifier in megahertz (MHz) WPT applications. The ODSV tracking enables the switches in the synchronous rectifiers work at the same switching operation with that of the diodes in the passive rectifiers. Thus, the soft-switching operation can be maintained with minimized body-diode conduction. A tracking algorithm is then developed to adaptively achieve the optimal operation of the synchronous rectifier under varying loading conditions. Finally, the proposed ODSV tracking scheme is implemented in a GaN-based Class E full-wave synchronous rectifier and tested in an experimental 6.78-MHz WPT system. A dc–dc efficiency of 91.6% is achieved under the output power of 120 W. The efficiency of the synchronous rectifier is 97.0% and the rectifier power density can be as high as 1212 W/in^3.**

***Index Terms*—Class E rectifier, megahertz (MHz) wireless power transfer (WPT), high power density, optimal drain–source voltage (ODSV) tracking, synchronous resonant rectifier.**

I. Introduction

WIRELESS power transfer (WPT) has become a promising candidate to charge everyday equipment, from cellphones to electric vehicles. In the past decade, this technology has attracted great interests from academia and industry. Comprehensive research work has been conducted on the WPT operating from kilohertz (kHz) to megahertz (MHz), and from low power levels (several watts) to high power levels (kWs) [1], [2]. It is known that increasing the operating frequency to MHz (for example, 6.78, 13.56, and 27.12 MHz) can achieve lighter and more compact WPT systems with higher spatial freedom. In addition, with loosely coupled coils, MHz WPT makes it possible to charge multiple devices simultaneously [3]. However, for the widespread use of MHz WPT, some problems still need to be solved, particularly its power conversion efficiency. Unlike the conventional plugged-in charging, when charging via the MHz WPT, high-frequency ac power is picked up and converted into dc power on the receiving side, usually an electronic device. The heating problem can be serious, especially for small-sized devices when the charging power is high. Meanwhile, in the conventional plugged-in charging, the dc power is directly provided to the electronic devices, and thus it is comparatively easier to increase the charging power.

The receiving side of the WPT system is usually embedded in an electronics device. It consists of a receiving coil and a rectifier. A receiving coil is generally desired to have a high quality factor. At the same time, improving the efficiency of rectifiers in MHz WPTs is more important and challenging due to the high-frequency switching operation. In a MHz WPT system, such as using a full-bridge rectifier, the power loss from the rectifier may become as high as four times the power loss from the receiving coil [4]. In order to further improve the rectification at MHz, the synchronous/active rectification has been studied in recent years [5]–[9]. The purpose is to minimize the conduction loss by replacing diodes with actively controlled switches, such as the gallium nitride (GaN) power switches. Existing work is mainly aimed at the application of biomedical implants, such as retinal prostheses or cochlear implants, whose power level is usually lower than a few watts, and most of rectifiers adopt a full-bridge topology mostly because of its simple circuit topology and high voltage conversion ratio. However, with a relatively high power level (such as tens or hundreds of watts) and a high operating frequency at MHz, the full-bridge rectifiers become less competitive due to their hard-switching property. Note that high-power switches usually have higher parasitics, resulting in longer turn-ON and turn-OFF times and severe switching losses for the bridge rectifiers operating at MHz [5], [6], [10]. In addition, the need for bootstrap gate drive circuits further reduces its applicability.

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The resonant rectifiers, such as Class E and Class EF rectifiers, have been known to be suitable for multi-MHz rectification thanks to their soft-switching operation and parasitic absorption capability [11]. For Class E/EF synchronous rectifiers, the parasitic drain–source capacitor can be absorbed into the shunt capacitor of the switch, which helps minimize parasitic ringing and improve rectification efficiency by reducing the harmonic contents [12]. Especially, the driving of synchronous resonant rectifiers with ground-referenced switches is easier than that of the synchronous bridge rectifiers requiring the bootstrap circuits to drive the high-side switches [10].

Targeting on a fixed nominal load, a 30-W Class E synchronous rectifier was built using the GaN power switches [13]. However, its efficiency apparently decreases when the actual load deviates from its nominal value. Adaptive time delay (ATD) control was proposed that achieved a 15-W 91.8% peak efficiency with a full-bridge synchronous rectifier in a 6.78-MHz WPT system [10]. Meanwhile, the ATD controller locks the time delay when the iteration completes. The operation of the rectifier cannot be dynamically adjusted afterward, such as when the loading condition changes. Delay-locked loop (DLL) was applied to compensate the turn-OFF delay and eliminate the leakage current of the full-bridge synchronous rectifier, again, in a 6.78-MHz WPT system [7]. Turn-ON delay, which can lead to extra conduction loss, is not compensated considering the low power level (below 6 W). With the DLL compensation, falling edge of gate driving voltage is aligned to the instant when rectifier input voltage crosses zero, whereas the additional turn-OFF delay of power switches, which is caused by the inherent Miller effects, is ignored. Four independent calibration circuits were used to compensate both turn-ON and turn-OFF delays of the switches in the full-bridge rectifier when loading condition changes, which helps achieve peak efficiency of 94.8% at a mW power level [8]. High reverse current occurs during start-up process, and thus may damage the switches in the full-bridge rectifier when the power level is high.

Different from the above existing work, this article studies synchronous resonant rectifiers and develops an optimal drain-source voltage (ODSV) tracking scheme to achieve efficient and adaptive MHz rectification for WPT applications. The purpose is to emulate near perfect diode, such as with zero parasitic capacitance. The ODSV is defined as the voltage with the same duty cycle and phase (i.e., the same turn-ON and turn-OFF instants) as the diode voltage in a corresponding passive rectifier. The advantages of the proposed ODSV tracking scheme are as follows.

1) Maintain the soft-switching operation of the switches, and naturally minimize the body-diode conduction.
2) Reach the optimal operation of the switches when the loading condition changes, and compensate the turn-ON/OFF delays of switches and propagation delays of detection and driving circuits.
3) Work for various synchronous resonant rectification topologies that use ground-referenced switches, such as Class E and Class EF topologies [14].

The remainder of this article is organized as follows. Section II investigates the diode voltage waveforms of three representative passive resonant rectifiers when the final load changes. Section III explains the hardware configuration to implement the ODSV tracking and operation modes of the synchronous resonant rectifiers, taking a Class E full-wave synchronous rectifier as an example. Then, Section IV discusses the principle of the ODSV tracking and the influences of the implementation errors. Section V experimentally validates the ODSV tracking scheme, both the tracking algorithm and hardware implementation, in which the synchronous rectifier demonstrates a high power density of 1212 W/in^3. Finally, Section VI draws the conclusion.

II. Resonant Rectifiers With a Varying Load

Fig. 1 shows three representative resonant rectifiers for the MHz WPT. In the figure, L_{rx} and C_{rx} are the self-inductance and compensation capacitor of the receiving coil. In the resonant rectifiers, the shunt capacitors (C_1, C_2, and C_r that absorb the corresponding parasitic capacitors) shape the diode voltages in such a way that the diodes achieve zero-voltage switching (ZVS) with low dv/dt [4], [12], [14]. Fig. 1(a) shows a current-driven Class E full-wave rectifier. It achieves high efficiency and low harmonics when the diode duty cycle is below 50%. In the Class EF_2 topology in Fig. 1(b), an LC resonant tank (i.e., L_{nd} and C_{nd}) is added in parallel that bypasses the second-harmonic component and thus suppresses the diode voltage stress [15]. A voltage-driven Class E rectifier is also shown in Fig. 1(c) [12].

Fig. 1(d)–(f) shows the simulated waveforms of the three rectifiers under a varying load R_L. Note that this variation in the final load is common in real applications. Here, the nominal R_L is 10 Ω and the amplitudes of the sinusoidal input current and voltage [i_{rx} in Fig. 1(d) and (e) and v_{rx} in Fig. 1(f)] are 1 A and 10 V, respectively. The diode voltage waveforms (red, coral, and orange curves) are plotted to show the influence of the varying R_L. The input current or voltage waveforms (blue curves) are also given for reference purposes. Only the waveforms of Q_1 in the Class E full-wave rectifier is shown in Fig. 1(d) because the waveforms of Q_2 are the same but in 180° phase difference. The waveforms in Fig. 1 clearly illustrate that the duty cycles and phases of the diode voltages in all the three rectifiers change with the varying load, which is from 5 to 50 Ω. Again, these natural changes in the duty cycle and phase essentially require adaptiveness in the switch control of the synchronous resonant rectifiers.

III. Configuration and Operation Modes

Based on the above discussion, the duty cycle and phase of the drain–source voltage of the switches in a synchronous resonant rectifier should adapt to the change in the final load. Therefore, an ODSV tracking scheme is proposed as follows. As shown in Fig. 1, the diodes in the passive resonant rectifiers always turn ON and OFF at the zero voltage with low dv/dt. Therefore, the waveforms of these diode voltages can serve as a reference to develop the control of the synchronous rectifiers. Here, the ODSV is defined as a voltage that emulates the same duty cycle and phase (i.e., the same turn ON and turn OFF instants) of the diode voltages in the corresponding passive rectifiers.

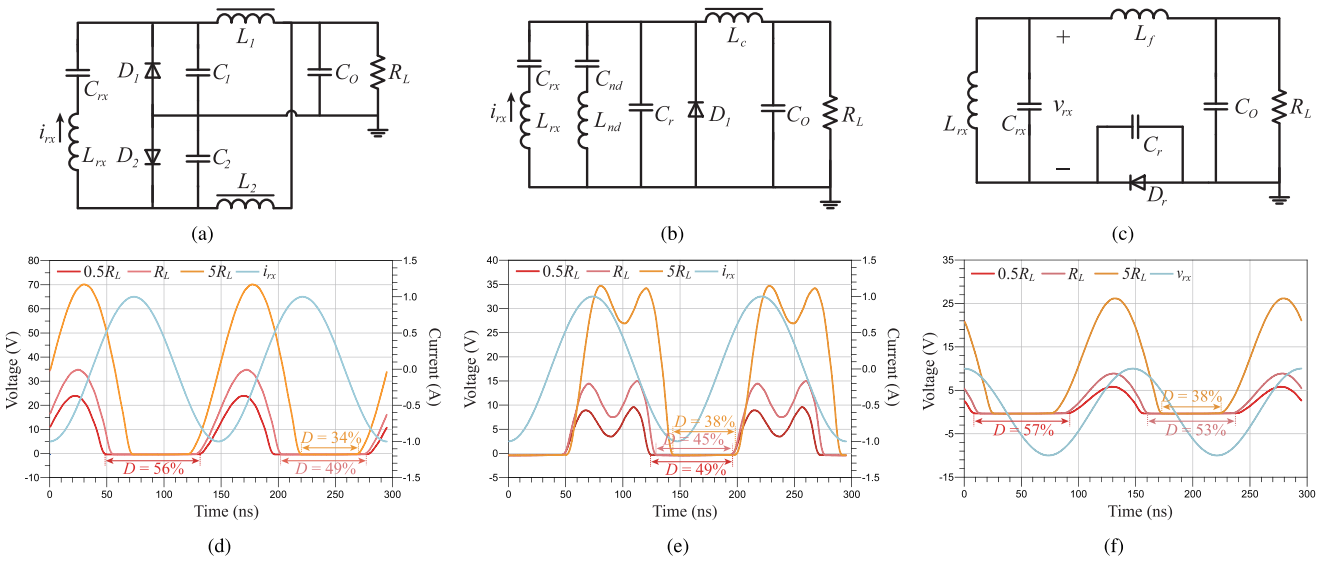


Fig. 1. Three representative resonant rectifiers. (a) Current-driven Class E full-wave rectifier. (b) Current-driven Class EF_2 rectifier. (c) Voltage-driven Class E rectifier. (d) Simulation waveforms of current-driven Class E full-wave rectifier. (e) Simulation waveforms of current-driven Class EF_2 rectifier. (f) Simulation waveforms of voltage-driven Class E rectifier.

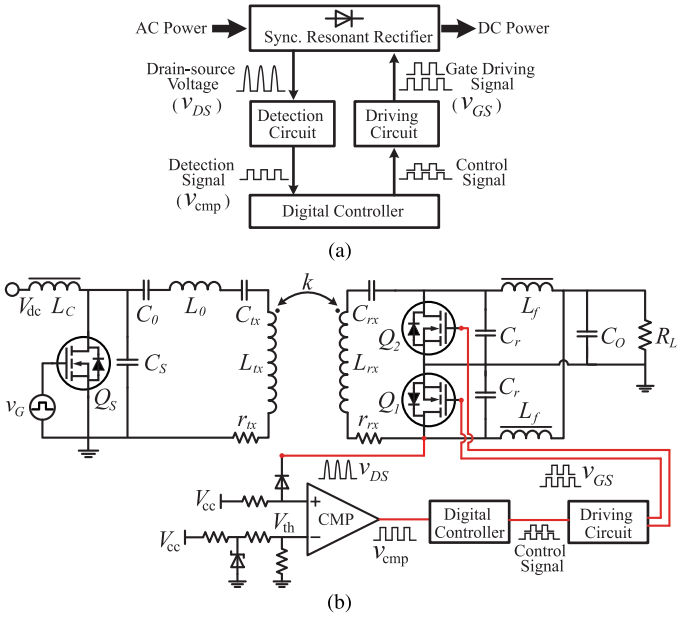


Fig. 2. System configuration of the ODSV tracking. (a) Block diagram. (b) Application in an example Class E full-wave synchronous rectifier.

Namely, the purpose of the ODSV tracking is to adaptively match the drain–source voltage waveforms of the switches in the synchronous resonant rectifiers to the diode voltage waveforms of their passive counterparts, which:

1) achieves the ZVS operation of the switches;
2) minimizes the body-diode conduction loss;

when the loading condition of the rectifiers changes.

A. Implementation Configuration

Fig. 2 shows the system configuration to implement the ODSV tracking. As shown in Fig. 2(a), the tracking system consists of a detection circuit, a digital controller, and a gate driving circuit. The synchronized detection signal includes the duty cycle and phase information of the switch drain–source voltage. The digital controller checks the change of the detection signal and adaptively generates the control signal, according to the ODSV tracking algorithm developed in Section IV-A. The gate driving signal is then generated based on the control signal.

Fig. 2(b) shows an example synchronous resonant rectifier with the proposed ODSV tracking system. Here, a single-ended Class E power amplifier (PA) is employed to drive the transmitting coil L_{tx}, and a current-driven Class E full-wave synchronous rectifier is applied on the receiving side [see Fig. 1(a)]. The ODSV tracking is then conducted as follows.

1) The detection circuit is implemented using a high-speed voltage comparator. The switch drain–source voltage v_{DS} is detected and compared with a threshold voltage V_{th} in order to generate the detection signal v_{cmp}. As will be explained Section IV-B, V_{th} is a small reference voltage that is slightly higher than zero.
2) Then, the digital controller checks change in v_{cmp} and accordingly generates two control signals with 180° out of phase that drive the two switches in the rectifier. Based on the real-time detection signal v_{cmp}, the digital controller adaptively adjusts the control signals to perform the ODSV tracking.

Note that this tracking scheme and circuit configuration are universal that can be extended to other high-frequency synchronous resonant rectifiers.

B. Analysis of Operation Modes

Fig. 3 gives the waveforms of the switch Q_1 in the above Class E full-wave synchronous rectifier that help understand the operation of the ODSV tracking. Fig. 3(a) and (b) shows the waveforms of the turn-ON and turn-OFF operations in one

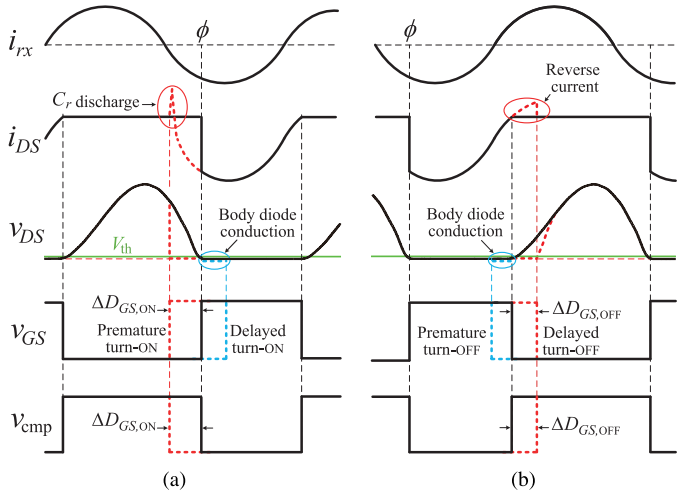


Fig. 3. Waveform illustration of the example Class E full-wave synchronous rectifier (black: optimal operation; blue: delayed turn-ON or premature turn-OFF; red: premature turn-ON or delayed turn-OFF). (a) Turn-ON operation. (b) Turn-OFF operation.

switching cycle, respectively. In these waveforms, i_{rx} is the rectifier sinusoidal input current; i_{DS} and v_{DS} are the switch drain-source current and voltage; V_{th} is the predefined threshold voltage; v_{GS} is the gate driving signal; and v_{cmp} is the detection signal that has the same phase and duty cycle with the drain–source voltage v_{DS}, neglecting the delay and error of the detection circuit. Different operation modes of the synchronous resonant rectifier are explained as follows.

1) *Optimal Operation (Black Solid Waveforms):* Both the ZVS operation and minimized body-diode conduction are simultaneously achieved. The turn-ON and turn-OFF instants of the gate driving signal v_{GS} are aligned with the timings when v_{DS} falls to zero or rises from zero. In this operation mode, the synchronous rectifier's drain–source-voltage waveforms (i.e., v_{DS}) well match with those of its equivalent passive counterpart.
2) *Body-Diode Conduction Operation (Blue Dash Waveforms):* Delayed turn-ON or premature turn-OFF occurs in the gate driving signal v_{GS}. Thus, i_{DS} flows through the switch body diode, which causes an additional conduction loss [refer to the two blue circles in Fig. 3(a) and (b)]. Meanwhile, the ZVS operation still maintains and the duty cycle of v_{cmp} or v_{DS}, i.e., D_{cmp} or D_{DS}, is the same as those in the above optimal operation.
3) *Hard-Switching Operation (Red Dash Waveforms):* Premature turn-ON or delayed turn-OFF occurs in the gate driving signal v_{GS}. The premature turn-ON operation shortens the shunt capacitor C_r, which leads to a fast discharge of C_r. v_{DS} suddenly drops to zero indicating the hard-switching operation, and the duty cycle of v_{cmp} or v_{DS} is reduced by $\Delta D_{GS,\text{ON}}$, as shown in Fig. 3(a). Similarly, the delayed turn-OFF operation causes the reverse current flowing through the switch and delays the charging of the shunt capacitor C_r. Again, the duty cycle of v_{cmp} or v_{DS} is reduced by $\Delta D_{GS,\text{OFF}}$.

From the above analysis, it can be seen that the duty cycle of the detection signal D_{cmp}, which is as same as D_{DS} if the implementation errors are neglectable, can be utilized to indicate if the hard-switching operation occurs. When D_{cmp} keeps unchanged with a varying gate driving signal, the synchronous rectifier works at optimal operation or body-diode conduction operation. In these two modes, D_{cmp} is almost the same with the duty cycle of the rectifying diodes in the passive rectifier. On the contrary, when D_{cmp} starts to decrease, the premature turn-ON or delayed turn-OFF happens and the rectifier works at hard-switching operation.

Fig. 4 shows the simulation results of the Class E full-wave synchronous rectifier when tuning the duty cycle of the gate driving signal (D_{GS}). The parameters $\Delta D_{GS,\text{ON}}$ and $\Delta D_{GS,\text{OFF}}$ (i.e., x and y axes in Fig. 4) are defined as the deviations of D_{GS} from its optimal turn-ON and turn-OFF instants [see Fig. 3]. When $\Delta D_{GS,\text{ON}}$ and $\Delta D_{GS,\text{OFF}}$ are both zero, the synchronous rectifier works at its optimal operation ($D_{DS} = 49\%$, $\eta_{\text{rec},Q} = 97.8\%$, $P_{R_L} = 100$ W). When delayed turn-ON ($\Delta D_{GS,\text{ON}} < 0$) or premature turn-OFF ($\Delta D_{GS,\text{off}} < 0$) occurs, the rectifier works at its body-diode conduction operation, as described in 2) in Fig. 4. Its D_{DS} keeps almost the same with that in the optimal operation, i.e., close to 49% [see Fig. 4(a)]. $\eta_{\text{rec},Q}$ slightly drops due to the body-diode conduction loss, and P_{R_L} is almost unchanged [refer to Fig. 4(b) and (c)]. Meanwhile, when premature turn-ON ($\Delta D_{GS,\text{ON}} > 0$) or delayed turn-OFF ($\Delta D_{GS,\text{OFF}} > 0$) happens, the rectifier works at the hard-switching operation, and D_{DS} becomes obviously smaller than that in the optimal operation and body-diode conduction operation [see Fig. 4(a)]. Hard-switching operation certainly deteriorates the rectifier efficiency and output power [see Fig. 4(b) and (c)]. The above simulation results show that the duty cycle of drain–source voltage (D_{DS}) can serve as an index of the present rectifier operation mode.

IV. ODSV Tracking

A. Operation Principle

Fig. 5 explains the start-up process of the ODSV tracking. Ideally the gate driving signal v_{GS} should be simply an inversion of the detection signal v_{cmp}. However, in real applications, implementation error is inevitable that leads to different duty cycles and phases between v_{cmp} and v_{DS} [see Fig. 2(a)]. This type of error also exists when generating v_{GS}, i.e., the implementation errors in the digital controller, driving circuits, and switches. Thus, the below feedback-based ODSV tracking is necessary and important. The analysis on this implementation errors is provided in the following section. Here, the error of the drain–source voltage detection is temporarily assumed to be zero. The start-up process of the ODSV tracking is then summarized as follows.

1) *Gate Driving Signal With a Small Duty Cycle:* At the beginning of the ODSV tracking, this driving signal (v_{GS}) is generated to guarantee that it completely locates at the ON-state of v_{DS}, as shown in Fig. 5(a). Due to the short conduction time interval of the switch, the synchronous rectifier works close to a passive rectifier but through its body diodes.

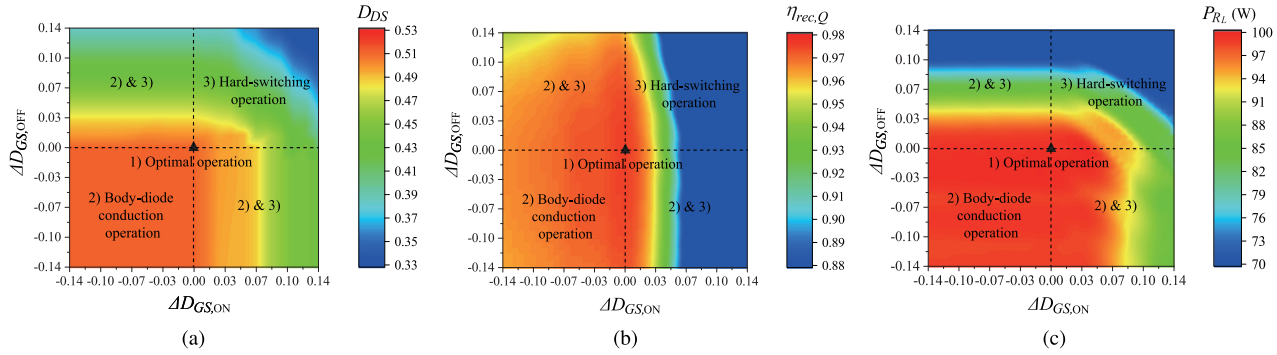


Fig. 4. Drain–source voltage duty cycle (D_{DS}), rectifier efficiency ($\eta_{\text{rec},Q}$), and load power (P_{R_L}) versus the duty cycle of gate driving signal (D_{GS}). (a) D_{DS}. (b) $\eta_{rec,Q}$. (c) P_{R_L}.

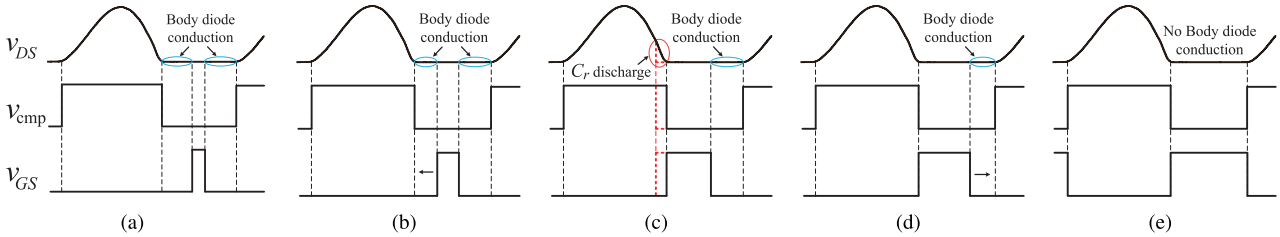


Fig. 5. Waveform illustration of the ODSV tracking start-up process. (a) Start from a small duty cycle. (b) Increase duty cycle D_{GS} toward turn-ON instant. (c) Reach the optimal turn-ON instant. (d) Increase duty cycle D_{GS} toward turn-OFF instant. (e) Reach the optimal turn-ON and turn-OFF instants.

2) *Perturbation Toward Optimal Turn-ON Instant:* A small and constant duty cycle perturbation toward the turn-ON instant, namely ΔD_{ON}, is then applied on v_{GS}. Thus, the duty cycle D_{GS} increases step by step until the turn-ON operation of the switches reach the optimal instant [see Fig. 5(b) and (c)]. At the same time, the drain–source voltage v_{DS} is monitored by observing the detection signal v_{cmp}. If the duty cycle D_{cmp} (D_{DS}) is unchanged, D_{GS} keeps increasing to reduce the body-diode conduction on the left side of the conduction interval while maintaining a fixed D_{cmp} (i.e., D_{DS}) [see Fig. 5(b)]. When the increasing D_{GS} leads to a decreased D_{cmp}, the rectifier operation transits from the optimal operation to the hard-switching operation. Thus, the highest D_{GS} that keeps D_{cmp} unchanged is the optimal value for the turn-ON operation of the switch [see Fig. 5(c)].

3) *Perturbation Toward Optimal Turn-OFF Instant:* Similarly, a small and constant duty cycle perturbation toward the turn-OFF instant, namely ΔD_{OFF}, can be applied on v_{GS}. Again, D_{GS} keep increasing in a step-by-step manner until D_{cmp} starts to decrease, namely the hard-switching operation. Thus, the last D_{GS} that keeps D_{cmp} unchanged is the optimal value for the turn-OFF operation of the switch [see Fig. 5(d) and (e)]. Note that the hard-switching here is not in the same way of the premature turn-ON that the shunt capacitor is shorted. Thus, the delayed turn-OFF is not as catastrophic but still lossy.

It should be noted that the optimal operation of the synchronous rectifier relies on the final load. Thus, the gate driving signal of the rectifier should be accordingly adjusted when the load varies. Therefore, the below iterative ODSV tracking

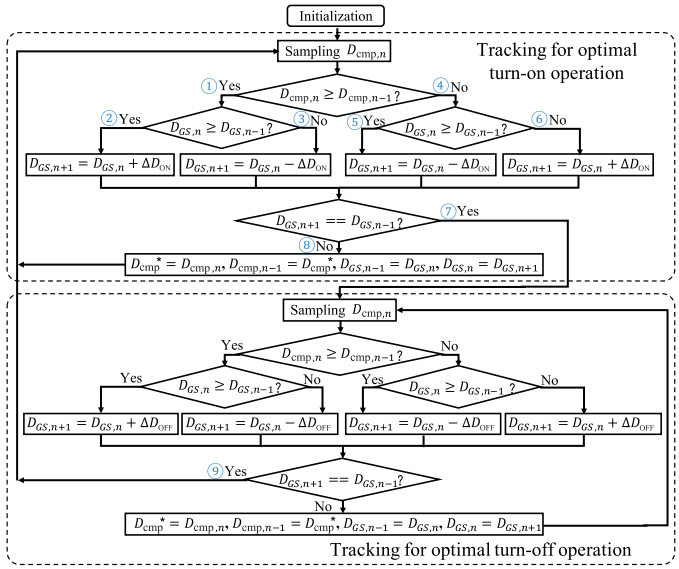


Fig. 6. Flowchart of the ODSV tracking algorithm.

algorithm in Fig. 6 is developed to adaptively achieve optimal operation of the rectifier under varying loading conditions. In the flowchart, $D_{\text{cmp},n-1}$ and $D_{\text{cmp},n}$ are the sampled drain–source voltage duty cycles in last round and present round; $D_{GS,n-1}$, $D_{GS,n}$, and $D_{GS,n+1}$ are the duty cycles of the gate driving signal in last, present, and next rounds; ΔD_{ON} and ΔD_{OFF} are the perturbations of the duty cycle toward the turn-ON instant and turn-OFF instant. As shown in Fig. 4(a), the tracking of optimal operation of the rectifier, i.e., the ODSV tracking, is

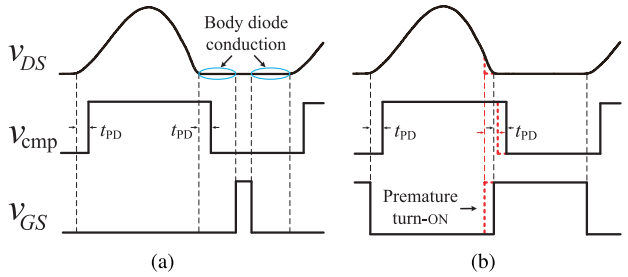


Fig. 7. Waveform illustration of the comparator propagation delay. (a) At the beginning of the tracking. (b) After the tracking.

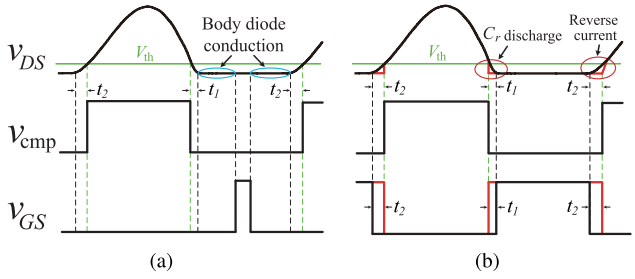


Fig. 8. Waveform illustration of the nonzero threshold voltage. (a) At the beginning of the tracking. (b) After the tracking.

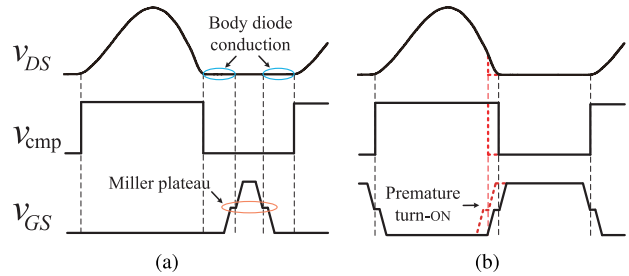


Fig. 9. Waveform illustration of the switch turn-ON/OFF delay. (a) At the beginning of the tracking. (b) After the tracking.

actually a convex optimization problem that can be solved via a two-dimensional hill-climbing algorithm.

1) *Tracking for Optimal Turn-ON Operation:* As shown in Fig. 6, if the detected D_{cmp} keeps unchanged or increases (①$D_{\text{cmp},n} \geq D_{\text{cmp},n-1}$), it indicates that the direction of tracking is desirable to reach the optimal operation of the synchronous rectifier. Thus, this direction of tracking, either a bigger (i.e., ②) or a smaller $D_{GS,n+1}$ (i.e., ③), should be maintained. On the contrary, if D_{cmp} decreases, the direction of tracking should be reversed, as shown in ④–⑥. Once the tracking of $D_{GS,n+1}$ converges (i.e., ⑦), the tracking for optimal turn-ON operation stops. Otherwise, the tracking continues (i.e., ⑧).
2) *Tracking for Optimal Turn-OFF Operation:* The tracking for the optimal turn-OFF operation is similar to that for the optimal turn-ON operation. When the rectifier reaches the optimal turn-OFF operation (namely ⑨$D_{GS,n+1} = D_{GS,n-1}$), the ODSV tracking shifts to the tracking for optimal turn-ON operation. Therefore, it is designed to iterate between the tracking for optimal turn-ON operation and the tracking for optimal turn-OFF operation in order to maintain optimal rectification efficiency.

Note that due to the discrete implementation, the synchronous rectifier may possibly operate with slight body diode conduction when the ODSV tracking is completed. Namely, the ODSV tracking always ensures at least a delayed turn-ON and premature turn-OFF to avoid the hard-switching, as shown in Fig. 5.

B. Implementation Error Analysis

When implementing the above ODSV tracking, the voltage comparator is used to generate the detection signal v_{cmp}. For safety purposes, the small threshold voltage V_{th} should be slightly higher than the drain–source voltage when the switch Q_1/Q_2 turns ON. Due to the comparator's inherent propagation delay and the nonzero threshold voltage, the phase and duty cycle of the detection signal v_{cmp} cannot be as same as the actual drain–source voltage v_{DS}. Implementation errors also exist in gate driving circuit and turn-ON/OFF of the switches. The influences of above hardware implementation errors are investigated as follows.

1) *Comparator Propagation Delay:* Fig. 7(a) and (b) shows the rectifier waveforms in one switching cycle. For illustrative purposes, the propagation delay is intentionally exaggerated. t_{PD} is the phase delay mainly caused by the comparator propagation delay. In the beginning of the ODSV tracking, the ZVS operation is achieved because the duty cycle of the gate driving signal D_{GS} is small, as shown in Fig. 7(a). Afterward, D_{GS} increases until the premature turn-ON happens and D_{cmp} starts to decrease [refer to the red dash waveform in Fig. 7(b)]. According to the principle of ODSV tracking, the last v_{GS} that keeps D_{cmp} unchanged is the optimal driving signal for the turn-ON operation of the switch. Therefore, through this tracking mechanism, the influence of the comparator propagation delay can be naturally compensated [refer to the black solid waveform in Fig. 7(b)].
2) *Nonzero Threshold Voltage:* The nonzero V_{th} causes the detection error in D_{DS}, the duty cycle of v_{DS}. Fig. 8(a) and (b) shows the waveforms, again, with an intentionally exaggerated threshold voltage to illustrate the influence. Here, t_1 and t_2 are the detection errors caused by the nonzero threshold voltage. The rising and falling edges of the detection signal v_{cmp} are consistent with the timing when v_{DS} crosses the threshold voltage, as shown in Fig. 8(a). The last v_{GS} that keeps D_{cmp} unchanged is shown by the red solid waveform in Fig. 8(b). It can be seen that the hard-switching slightly happens due to the premature turn-ON and delayed turn-OFF of the switch. This deteriorates the efficiency. In real applications, proper printed-circuit-board (PCB) design helps reduce the noise overlaid on v_{DS}, and thus V_{th} can be chosen to be sufficiently small to minimize the detection error.
3) *Switch Turn-ON/OFF Delay:* The actual switches, such as MOSFETs, certainly take time to turn ON and turn OFF due to the well-known Miller effect. As shown in Fig. 9(b), during the ODSV tracking, the duty cycle of the gate driving signal D_{GS} increases until the premature turn-ON

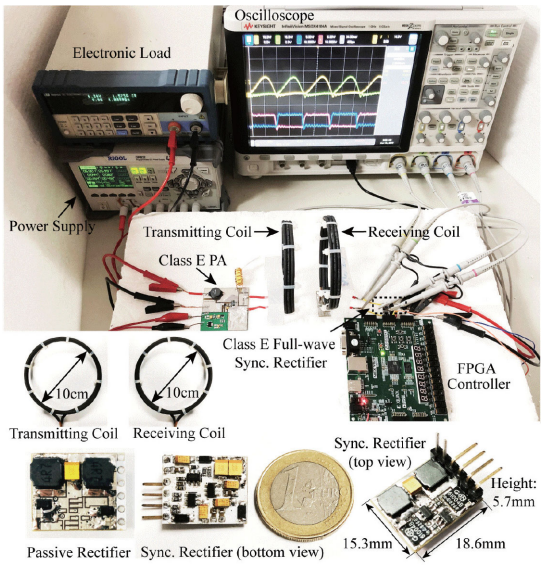


Fig. 10. Experimental setup of the 6.78-MHz WPT system using the Class E full-wave synchronous/passive rectifiers.

occurs [see the red dash waveform]. Thus, the previous D_{GS} is taken as optimal. In the same subfigure, the corresponding optimal v_{GS} after the tracking turns ON the switch, aligning with the timing when the Miller plateau ends [see the black solid waveform]. Similarly, for the turn-OFF operation, it also conducts at the beginning of the Miller plateau. Therefore, the proposed ODSV tracking also adapts with the existence of the switch turn-ON/OFF delay.

In general, the proposed ODSV tracking scheme can adaptively compensate the adverse influences of the circuit propagation delay and the switch turn-ON/OFF delay. Note that the analysis of gate driving circuit delay is similar to that of switch turn-ON/OFF delay and thus is omitted here. This tracking scheme is a universal approach that can be applied in other synchronous resonant rectifiers operating at high frequencies. Such applications are usually quite sensitive to the hardware time delays. A simpler method of using a comparator to both detect and generate the control signals is difficult to work properly at high operating frequencies and high power levels due to its inflexibility to handle the hardware time delays.

V. Experimental Verification

A. Setup and Configuration

An experimental 6.78-MHz WPT system has been built for verification purposes, as shown in Fig. 10. The system uses either the Class E full-wave synchronous rectifier or its passive counterpart to investigate the improvements. The circuit configuration of the experimental system is given in Fig. 2(b), which uses the synchronous rectifier. The experimental system consists of a Class E PA, a pair of coupling coils, and a Class E full-wave synchronous/passive rectifier. The electronic load in Fig. 10 emulates the final dc load and measures the output power. Two 45-A 100-V GaN power switches from GaN Systems, GS61004B, are used in the synchronous rectifier mostly due to their low ON-resistances. The synchronous rectifier was fabricated with a four-layer PCB and 1 mm in thickness. The ODSV tracking algorithm is implemented using a high-speed field programmable gate array (FPGA) control board, Digilent Nexys 4 operating at 500 MHz clock frequency. The transmitting coil and receiving coil are separated with a distance of 3 cm (the mutual inductance coefficient $k = 0.177$). Equivalent series resistances of the coupling coils, i.e., r_{tx} and r_{rx}, are both 0.16 Ω. The coupling coils are designed to be fully resonant, considering the nonzero reactance of the rectifier [11]. Therefore, the load seen by the Class E PA is pure resistive. The PA parameters are then determined based on its nominal load and Raab's equations [16]. A 15-A 650-V GaN power switch GS66504B, again from GaN Systems, is used in the Class E PA. The major parameters of the experimental system are summarized in Table I. Note that parasitic capacitances of the power switches are absorbed into the capacitances of the corresponding external capacitors, i.e., C_S and C_r. Note that practically the mismatch between MOSFETs and resonant components can result in different optimal duty cycles of the two-channel gate driving signals, and their optimal phase difference is no longer 180°. In present experiments, the ODSV tracking only guarantees the optimal operation of one of the two MOSFETs, such as Q_1 in Fig. 2(b), because of the direct sampling of its drain–source voltage. Therefore, the body-diode conduction or hard-switching operation may occur in another MOSFETs Q_2, resulting in reduced efficiency. The mismatch may also lead to different voltage and current stresses of the two MOSFETs and shunt capacitors. The total harmonic distortion and electromagnetic interference performance of the rectifier could deteriorate too. The mismatch may be caused due to the different parasitic capacitances of the MOSFETs, errors in shunt capacitors, asymmetrical routing, and layout of PCB. In practice, the shunt capacitors C_r with low tolerance (such as within ±1%) is preferred. The Class E full-wave passive rectifier was also designed and fabricated for comparison purposes. It uses two 3-A 100-V Schottky diodes, V3FM10, from Vishay Intertechnology. The parameters of the WPT system using the passive rectifier were also accordingly designed.

TABLE I
Parameters in Experimental System

ω	C_S	C_0	L_0	C_{tx}
6.78 MHz	150 pF	1540 pF	1.12 μH	324 pF
L_{tx}	r_{tx}	C_{rx}	L_{rx}	r_{rx}
1.70 μH	0.16 Ω	374 pF	1.67 μH	0.16 Ω
k	C_r	R_L	-	-
0.177	1000 pF	4 Ω	-	-

B. Efficiencies Versus Output Powers

First, a fixed load, $R_L = 4$ Ω, is adopted. Fig. 11 shows the rectifier efficiency and system efficiency versus different output powers, during which the PA input voltage is adjusted to meet the required output power. The parameters $\eta_{\text{rec},Q}$ and

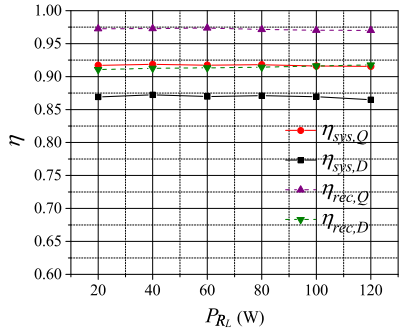


Fig. 11. Rectifier efficiency and system efficiency versus output powers.

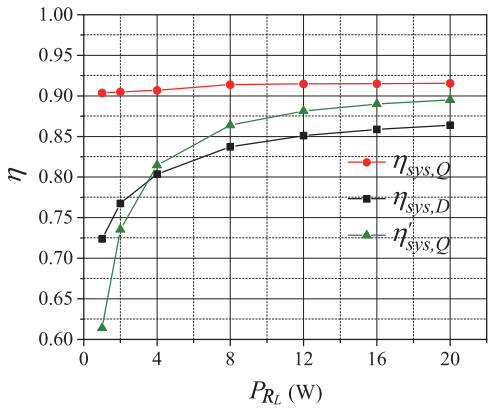


Fig. 12. System efficiency under low output powers.

$\eta_{\text{rec},D}$ are the efficiencies of the synchronous rectifier and the passive rectifier, respectively; similarly, $\eta_{\text{sys},Q}$ and $\eta_{\text{sys},D}$ are the dc–dc efficiencies of the two 6.78-MHz WPT systems. $\eta_{\text{rec},Q}$ maintains between 97.0%–97.4% when output power varies. When the output power is 120 W, the corresponding WPT system can reach 97.0% rectifier efficiency ($\eta_{\text{rec},Q}$) and 91.6% dc–dc efficiency ($\eta_{\text{sys},Q}$). Meanwhile, using the passive rectifier achieves efficiencies of 91.7% ($\eta_{\text{rec},D}$) and 86.5% ($\eta_{\text{sys},D}$). With the 120 W output power, the power density of the synchronous rectifier is 1212 W/in^3.

Fig. 12 shows the dc–dc system efficiency under low output powers. Here, the rectifier efficiency is not directly provided because of the inaccurate measurement of the ac power at low power levels. Note that $\eta'_{\text{sys},Q}$ (i.e., the green curve) is the system efficiency considering the 0.5-W driving loss of the synchronous rectifier. It can be seen that the synchronous rectifier is not needed when the output power is less than 3 W.

To further validate the improved efficiency of the synchronous rectifier, the thermal images of the synchronous and passive rectifiers are captured and compared in Fig. 13 (25 °C room temperature). For safe operation of the rectifiers, a cooling fan with wind speed of 390 LFM is used during the test. First, the two rectifiers are tested with the same 60 W output power. It can be seen that the temperatures of the GaN power switches are about 49–50 °C, only about half of the diode temperatures, i.e., 105–115 °C. The synchronous rectifier clearly demonstrates an improved efficiency. Meanwhile, the filter inductors L_f in a passive rectifier are obviously heated up by the nearby diodes. Second, the synchronous rectifier is also tested under 120 W output power. The temperatures of the power switches are below 70 °C, which shows the high efficiency and high power density of the synchronous rectifier.

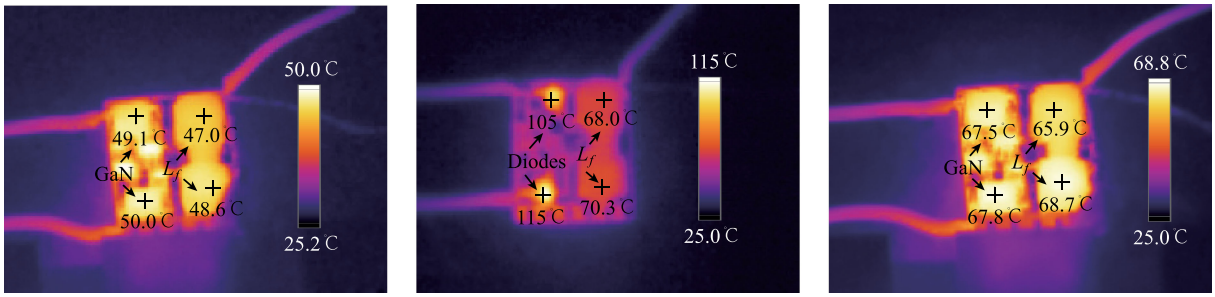
C. Efficiencies Versus Loads

Fig. 14 shows the rectifier and system efficiencies versus different loads R_L. The load of the rectifier is swept from 4 to 28 Ω. Again, the PA input voltage is adjusted accordingly to provide a constant output power, i.e., 20 W. The results show that $\eta_{\text{rec},Q}$ maintains between 97.0%–97.6% when R_L varies. $\eta_{\text{rec},D}$ slightly increases when load increases. It is about 4%–6% lower than $\eta_{\text{rec},Q}$. Due to the largely changing R_L, both $\eta_{\text{sys},D}$ and $\eta_{\text{sys},Q}$ obviously decrease mostly due to the undesired Class E PA loading condition. Note that the PA performance degradation (such as efficiency) can be mitigated by adding a impedance matching network that improves the PA loading condition when the final load changes [3].

To further investigate the ODSV tracking performance, the waveforms of the synchronous rectifier are captured when the load R_L changes. Fig. 15 shows the waveforms of v_{DS} and v_{GS} when R_L changes from 24 to 4 Ω. When the load changes, it takes about 16.5 ms for the synchronous rectifier to complete the ODSV tracking. A smaller R_L results in a smaller D_{DS} and thus a higher D_{GS}. Under all the different R_Ls, the ODSV tracking is well achieved. From Fig. 15, it can be seen that the turn-ON (rising) and turn-OFF (falling) instants of the gate driving signal v_{GS} always align with the timings when the voltage v_{DS} drops to zero and rises from zero, respectively, when the load changes. Therefore, the body-diode conduction of the power switches is minimized while the soft-switching is well preserved. These waveforms well validate the proposed ODSV tracking for the synchronous resonant rectifier. Note that the ODSV tracking naturally takes a period of time to converge. At the same time, the achievable response time is also largely determined by the speed of implementation. For the present experimental setup, there is further room to speed up the response time, such as through improved FPGA hardware programming. Fast possible implementation is especially important for the applications where large load steps frequently occur, because it shortens the transition time from hard-switching operation to body-diode conduction operation or optimal operation.

D. Loss Breakdown

For a system-level comparison, Table II lists the loss breakdown of the two WPT systems using the synchronous and passive rectifiers with 4-Ω load and 120 W output power. The power loss occurs in the passive rectifier is the largest source of the power loss in the WPT system, 57.8% of the total power loss. This power loss from the rectifier is especially challenging because a high thermal dissipation will occur on the receiving side such as a mobile device. It also justifies the importance of further improving the rectifier efficiency. By using the synchronous



(a) (b) (c)

Fig. 13. Thermal images of the synchronous and passive rectifiers. (a) Synchronous rectifier (60-W P_{R_L}). (b) Passive rectifier (60-W P_{R_L}). (c) Synchronous rectifier (120-W P_{R_L}).

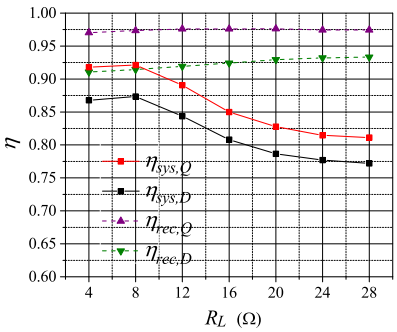


Fig. 14. Rectifier and system efficiency versus load.

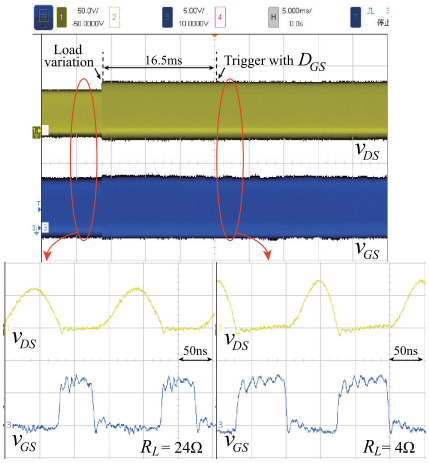


Fig. 15. Experimental waveforms of v_{DS} and v_{GS} when load changes.

TABLE II
LOSS BREAKDOWN WITH 4-Ω R_L AND 120-W P_{R_L}

Losses	WPT system#1 (Sync. Rec.)	WPT system#2 (Passive Rec.)
Rectifier	3.7 W	10.8 W
Receiving Coil	2.0 W	2.2 W
Transmitting Coil	0.9 W	1.0 W
Class E PA	4.4 W	4.7 W
Driving Loss	0.5 W	-
Total	11.5 W	18.7 W

rectifier, the power loss from the rectifier is significantly reduced by 61.1%, even considering its additional driving loss.

In terms of the overall system, the 6.78-MHz WPT system using the synchronous rectifier saves 7.2 W power losses in total with the 120 W output power.

VI. CONCLUSION

This article develops a universal ODSV tracking scheme for synchronous resonant rectifiers in MHz WPT applications. The key of ODSV tracking is to closely match the switch drain–source voltage waveform of the synchronous rectifier to the diode voltage waveform of the passive rectifier to naturally achieve soft-switching operation and minimize body-diode conduction. Based on this principle, a tracking algorithm is developed that adaptively achieves the optimal operation of the synchronous rectifier under a varying loading condition. The ODSV tracking scheme is experimentally validated by the Class E full-wave synchronous rectifier in a 6.78-MHz WPT system. A dc–dc efficiency of 91.6% and a rectifier efficiency of 97.0% are observed at 120-W output power. The power density of the synchronous rectifier can be as high as 1212 W/in^3. The developed ODSV tracking scheme is universal for various high-frequency synchronous resonant rectifiers. This article mainly focuses on the operation principle of the ODSV tracking and its experimental verification. The stability analysis using the small signal model will be an important future work.

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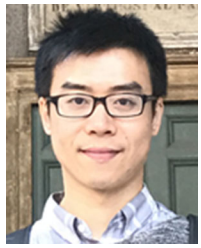

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